LISTING OF THE CLAIMS

Claim 1 (Currently Amended) A method of forming an integrated semiconductor circuit comprising the steps of:

providing a silicon-on-insulator structure comprising at least a top semiconductor layer located on a buried insulating layer, said top semiconductor layer having at least one patterned hard mask located in a FinFET region of the structure and at least one patterned hard mask located in a FET region of the structure;

protecting the FET region and trimming the at least one patterned hard mask in said FinFET region, wherein each trimmed patterned hard mask in said FinFET region has a horizontal surface whose width is less than the width of that of each patterned hard mask in said FET region;

etching exposed portions of the top semiconductor that are not protected with said hard masks stopping on said buried insulating layer, said etching defining a FinFET active device region and a FET active device region, said FinFET active device region being perpendicular to the FET active device region;

protecting the FinFET active device region and thinning the FET active device region so that the FET device region has a height that is less than the height of the FinFET active device region;

forming a gate dielectric on each exposed vertical surface of the FinFET active device region, while forming a gate dielectric on an exposed horizontal surface of the FET device region; and

forming a patterned gate electrode on each exposed surface of the gate dielectric.

Claim 2 (Original) The method of Claim 1 further comprising forming spacers abutting the patterned gate electrode.

Claim 3 (Original) The method of Claim 1 wherein said patterned hard masks are formed by the steps of: forming an oxide layer on a surface of the top semiconductor layer; forming a cap layer on the oxide layer; applying a photoresist to an exposed surface of the cap layer; exposing the photoresist to a pattern of radiation; developing the pattern into the photoresist; and transferring the pattern from the photoresist into the cap layer and the oxide layer.

Claim 4 (Original) The method of Claim 1 wherein the protecting the FET region comprising applying a resist mask to the FET region.

Claim 5 (Original) The method of Claim 1 wherein said trimming includes a chemical oxide removal process or a wet etch process.

Claim 6 (Original) The method of Claim 1 wherein the FinFET active device region has a (110) surface orientation and the FET active device region has a (100) surface orientation.

Claim 7 (Original) The method of Claim 1 wherein the protecting the FinFET active device region comprises applying a resist mask to the FinFET active device region.

Claim 8 (Original) The method of Claim 1 wherein the FinFET active device region has a (100) surface orientation and the FET device region has a (110) surface orientation.

Claim 9 (Original) The method of Claim 1 wherein said thinning includes an etching process that is highly selective to SiO_2.

Claim 10 (Original) The method of Claim 1 wherein said gate dielectric is an oxide formed by a thermal oxidation process.

Claim 11 (Original) The method of Claim 1 wherein said patterned gate electrodes are formed by depositing a gate conductor material; forming a patterned resist on top of the gate conductor material; and etching exposed portions of the gate conductor not protected with the patterned resist.

Claim 12 (Withdrawn) An integrated semiconductor circuit comprising:

at least one FinFET and at least one planar single gated FET located atop a buried insulating layer of an silicon-on-insulator substrate, said at least one planar single gated FET comprising an active device region that includes a patterned top semiconductor layer of the silicon-on-insulator substrate and said at least one FinFET has a vertical channel that is perpendicular to the at least one planar single gated FET.

Claim 13 (Withdrawn) The integrated semiconductor circuit of Claim 12 wherein the top semiconductor layer is comprised of Si.

Claim 14 (Withdrawn) The integrated semiconductor circuit of Claim 12 wherein the buried insulating layer is comprised of an oxide.

Claim 15 (Withdrawn) The integrated semiconductor circuit of Claim 12 wherein the vertical channel has a height that greater than the patterned top semiconductor layer of the at least one planar single gated FET.

Claim 16 (Withdrawn) The integrated semiconductor circuit of Claim 12 wherein the vertical channel has a (110) surface orientation, and the at least one planar single gated FET has a (100) surface orientation.

Claim 17 (Withdrawn) The integrated semiconductor circuit of Claim 12 wherein the at least one FinFET is a double gate device.

Claim 18 (Withdrawn) The integrated semiconductor circuit of Claim 12 wherein the vertical channel has a (100) surface orientation, and the at least one planar single gated FET has a (110) surface orientation.